Internal Qualification & Reliability Report

SDRAM

512Mb

32 Meg × 16

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VDD Transfer Characteristics

Alliance Memory's 512Mb SDRAM has an on-chip voltage regulator that is activated when the internal voltage of the device reaches a given level. The internal voltage of the device depends upon the voltage applied externally. The transfer characteristics of Alliance Memory's 512Mb SDRAM is depicted below. To ensure functionality, the on-chip voltage regulator is checked during back-end testing.

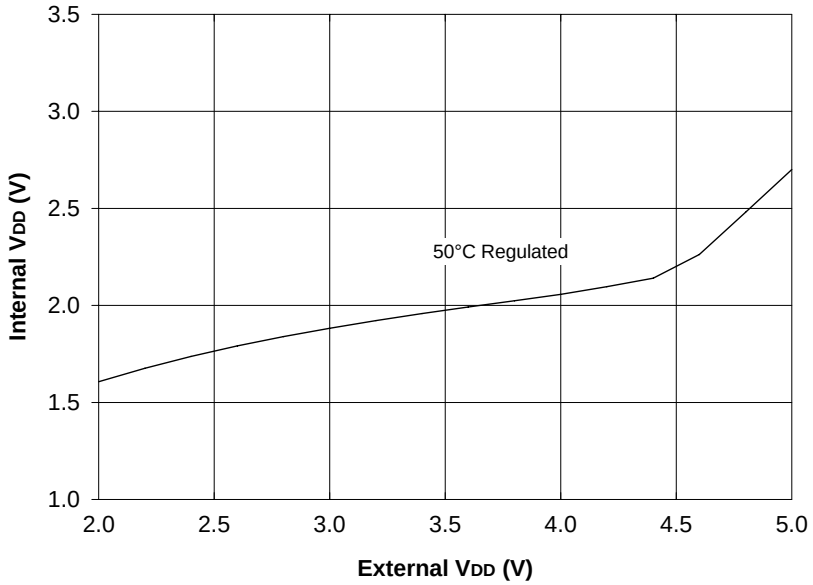

Figure 1: Internal versus External VDD Levels for 3.3V device, 50°C

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Reliability Test Results Summary

Table 1: Summary — Reliability Test Results

The package reliability data presented in this report represent both Pb-free and SnPb part numbers. Alliance Memory has determined that the intrinsic package reliability perfor-mance of Pb-free and SnPb are equivalent.

TEST NAME and CONDITIONS	HOURS or CYCLES (Failures/Devices Tested)					
HIGH TEMPERATURE OPERATING LIFE 125°C, 2.3V V_{DD} internal, dynamic pin bias, checker- board and checkerboard-complement patterns. Typical Operating Conditions (50°C, 3.3V): 4 FITs	**168 Hrs**	**336 Hrs**	**504 Hrs**	**672 Hrs**	**840 Hrs**	**1008 Hrs**
	0 / 600	0 / 600	0 / 600	0 / 600	0 / 600	0 / 600
LOW TEMPERATURE OPERATING LIFE –10°C, 2.3V V_{DD} internal, dynamic pin bias, checker- board and checkerboard-complement patterns.	**168 Hrs**	**336 Hrs**	**504 Hrs**	**672 Hrs**	**840 Hrs**	**1008 Hrs**
	0 / 89	0 / 89	0 / 89	0 / 89	0 / 89	0 / 89
HIGHLY ACCELERATED STRESS TEST 130°C, 85% RH, 33.3 psia, 1.95V on alternating balls	**96 Hrs**					
	0 / 230					
TEMPERATURE CYCLE –55°C for 15 minutes, +125°C for 15 minutes, air to air	**250 Cycles**	**500 Cycles**	**750 Cycles**	**1000 Cycles**		
	0 / 230	0 / 230	0 / 230	0 / 230		
HIGH TEMPERATURE STORAGE 150°C, no bias	**504 Hrs**		**1008 Hrs**			
	0 / 240		0 / 240			
MOISTURE SENSITIVITY LEVEL 260°C reflow	Level 4					
SOLDERABILITY 215°C peak reflow temperature, FR4 substrate, LO SnPb solder paste	0 / 15					
BOND INTEGRITY (minimum gmf)	**Gold Bond Shear**		**Wire Pull**			
	23.8 gmf		6.0 gmf			
ELECTROSTATIC DISCHARGE Minimum	**HBM**	**MM**	**CDM**			
	>2,000V	>200V	>1,000V			
I/O LATCH-UP $I_{Trigger}$ at 85°C	>150mA					

Note: Alliance Memory references JEDEC standard JESD47 when conducting reliability tests for the qualification of new products.

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High Temperature Operating Life

Sample Size: A minimum of 3 production lots are used for this test.

Preconditioning: Devices were run three times through a convection reflow oven, reaching a peak temperature of 260°C.

Test conditions: 125°C, 2.3V V_{DD} internal, dynamic pin bias, checkerboard and checkerboard-complement patterns for 1,008 hours in 168-hour intervals. Devices are tested for functionality after each interval. Alliance Memory references JEDEC standard JESD22 when conducting HTOL testing.

Failure rate at 60% confidence level: Using the test results provided in Table 2 and the calculation method provided below, the estimated failure rate for Alliance Memory's 512Mb SDRAM is 4 FITs (failures in time per billion device hours). Assumptions used in calculating this FIT rate were:

- Pn = 0.916
- Ea = 0.6eV
- Device Hours = 6.048×10^5
- ß = 5
- $AF_{overall} = 429$

Calculation of this hard error FIT rate estimate assumes typical operating conditions of 3.3V V_{DD}, 50°C. The actual FIT rate in a specific application may materially differ from this estimate, based on the actual operating conditions.

Table 2: HTOL Test Results

168 Hours	336 Hours	504 Hours	672 Hours	840 Hours	1,008 Hours
0 / 600	0 / 600	0 / 600	0 / 600	0 / 600	0 / 600

Failure Rate Calculation

Alliance Memory used the following model to calculate device failure rate.

$$\text{Failure Rate} = \frac{\text{Pn}}{\text{Device hours accelerated environment} \times \text{AF relative to typical operating environment}}$$

where:

Pn = Poisson Statistic (at a given confidence level).

Device Hours= Sample size multiplied by test time (in hours).

AF = Acceleration Factor between the stress environment and typical operating conditions.

To state the failure rate in FITs, we multiply the failure rate obtained from the equation above by 10^9.

Acceleration Factor Calculation

The acceleration factor between the internal voltage and internal temperature of the device during HTOL stress conditions and during typical operating conditions is computed using the following two models:

1. Acceleration factor due to temperature stress:

$$AF_T = e^{\frac{E_a}{k}\left[\frac{1}{T_o} - \frac{1}{T_s}\right]}$$

where: k = Boltzmann's constant = 8.617×10^{-5} eV/K.

T_o and T_s = Typical operating and stress temperatures, respectively, in kelvins.

E_a = Activation energy in eV.

2. Acceleration factor due to voltage stress:

$$AF_V = e^{\beta\langle V_S - V_O\rangle}$$

where:

V_s and V_o = Stress voltage and operating voltage.

ß = Constant equal to the slope of failure time ($t_{50\%}$) versus applied stress, derived from experiments conducted by Alliance Memory.

The overall acceleration factor due to temperature and voltage stress is calculated as the product of the temperature and voltage acceleration factors:

$$AF_{overall} = AF_{temperature} \times AF_{voltage}$$

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Low Temperature Operating Life

Sample Size: A minimum of 3 production lots are used for this test.

Preconditioning: Devices are run three times through a convection reflow oven, reaching a peak temperature of 260°C.

Test conditions: –10°C, 2.3V V_{DD} internal, dynamic pin bias, checkerboard and checkerboard-complement patterns for 1,008 hours in 168-hour intervals. Devices are tested for functionality after each interval. Alliance Memory references JEDEC standard JESD22 when conducting LTOL testing.

Table 3: LTOL Test Results

168 Hours	336 Hours	504 Hours	672 Hours	840 Hours	1,008 Hours
0 / 89	0 / 89	0 / 89	0 / 89	0 / 89	0 / 89

Highly Accelerated Stress Test

Sample Size: A minimum of 3 production lots are used for this test.

Preconditioning: Devices are soaked to their rated moisture sensitivity level and run three times through a convection reflow oven, reaching a peak temperature of 260°C.

Test conditions: 130°C, 85% RH, 33.3 psia, 1.95V on alternating balls. The test is conducted for 96 hours. Devices are tested for functionality after 96 hours of stressing. Alliance Memory references JEDEC standard JESD22 when conducting HAST testing.

Table 4: HAST Test Results

Package	96 Hours
54L TSOP	0 / 230

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Temperature Cycle

Sample Size: A minimum of 3 production lots are used for this test.

Preconditioning: Devices are soaked to their rated moisture sensitivity level and run three times through a convection reflow oven, reaching a peak temperature of 260°C.

Test conditions: –55°C (15 minutes), +125°C (15 minutes), air to air, no bias. Devices are exposed to 1,000 cycles at 250-cycle intervals and are tested for functionality after each interval. Alliance Memory references JEDEC standard JESD22 when conducting TC testing.

Table 5: T/C Test Results

Package	250 Cycles	500 Cycles	750 Cycles	1000 Cycles
54L TSOP	0 / 230	0 / 230	0 / 230	0 / 230

High Temperature Storage

Sample Size: A minimum of 3 production lots are used for this test.

Preconditioning: Devices are run three times through a convection reflow oven, reaching a peak temperature of 260°C.

Test conditions: 150°C, unbiased for 1008 hours in 504-hour intervals. Devices are tested for functionality after each interval. Alliance Memory references JEDEC standard JESD22 when conducting HTS testing.

Table 6: HTS Test Results

Package	504 Hours	1008 Hours
54L TSOP	0 / 240	0 / 240

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Electrostatic Discharge

Alliance Memory's ESD test circuit setup and waveforms for Human Body Model testing are in accordance with ESDA STM 5.1, MIL-STD-883, test method 3015 and JEDEC standard JESD22-A114B requirements, where applicable.

Micron's conducts Machine Model testing in accordance with ESDA STM 5.2 and JEDEC standard JESD22-A115A requirements, where applicable.

Alliance Memory conducts Charged Device Model testing in accordance with ESDA-SP 5.3.2 socketed device model standard practice requirements.

Six samples per ESD stress levels taken from three different production lots were tested for leakage, standby current, and functionality. The samples are tested at room temperature. All samples passed HBM, MM, and CDM tests.

Table 7: ESD Test Results

Leads	Minimum (V)		
	HBM (≥ class 2)	MM (≥ class B)	CDM (SDM)
Address	>2,000	>200	>1,000
Control	>2,000	>200	>1,000
Data	>2,000	>200	>1,000
Power	>2,000	>200	>1,000
Ground	>2,000	>200	>1,000

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Latch-Up

Latch-up is a destructive phenomenon that can occur in CMOS circuits. When latch-up occurs, the power supply voltage collapses and a low-resistance path between the power and ground supplies is established. This condition results in excessive current flowing through the internal circuits of the device, and can cause either functional or high standby current failures.

CMOS technology results in the presence of complementary parasitic bipolar transistors (that is, PNP and NPN devices). These parasitic bipolar transistors can form unwanted lateral PNPN structures, which can behave like a silicon-controlled rectifier (SCR). After the SCR triggers and snaps back, its behavior is similar to a diode. However, an external voltage or stimulus is required to trigger conduction of the parasitic SCR device.

Latch-up occurs after a parasitic SCR structure is triggered into conduction, typically as a result of improper device operation (for example, operation in excess of specification limits). Latch-up susceptibility is characterized using two distinct test methods: 1) V_{DD} overvoltage latch-up test method and 2) input/output current injected test method.

Overvoltage Latch-Up V_{DD} Test

Alliance Memory's operational latch-up test for V_{DD} overvoltage uses an external power supply and an ammeter to monitor the I_{DD} current. A static latch-up test is performed in both a standby and operating mode per the device's datasheet. Typically, the device is exercised using READ-WRITE cycles with a checkerboard pattern. V_{DD} is increased to progressively larger voltages until the device either latches or reaches the maximum current injection limits of 200mA or the maximum voltage compliance limit (1.5x V_{DD}_max). Power supply voltages are recorded just prior to the device reaching those limits. V_{DD} is decreased back to normal operating voltage (V_{DD} nominal). The overvoltage latch-up V_{DD} test results provided in the following table represent 6 samples from 3 different production lots.

Table 8: Overvoltage Latch-Up V_{DD} Test Results

Power Pins	Volts
V_{DD}	>5.4
V_{DDQ}	>5.4
Note: Tested at 25°C and 85°C in operating and standby modes.	

I/O Latch-Up Current Injected Test

Negative and positive input/output current injected tests are performed on all nonpower-supply leads† in accordance with JEDEC standard JESD78. A trigger source is used to sink current out of the device. Initially, the device under test is powered up to V_{DD}_max voltage as specified for the product. Excluding the lead under test, all input/bi-directional leads are tested for both max logic high and min logic low; all output leads are left floating. A current-trigger pulse is then applied to the lead under test for 1s. The device is allowed to cool down for 1s before the lead under test is again pulsed. The exact details of the current-trigger pulse waveform are shown in Figure 2 on page 8.

The power-supply current is measured approximately 500ms after the current trigger pulse. Latch-up has occurred if the power-supply current is 1.4x Inom or Inom + 10mA, whichever is greater. Data provided in Table 9 represent 6 samples from 3 different production lots.

Table 9: I/O Latch-Up Current Injected Test Results

Lead Name	$I_{Trigger}$ (mA) at 85°C
	Minimum
Address	>150
Control	>150
A12 (High Voltage Lead)	>150
Data	>150

Test sequencing is performed by applying a single current trigger pulse to each lead, starting at 50mA. Current pulse magnitudes are progressively increased in either +50mA or -50mA steps until all leads have been characterized for latch-

† The term "ball," rather than "lead," is applicable in this discussion when the device being tested is in an FBGA package.

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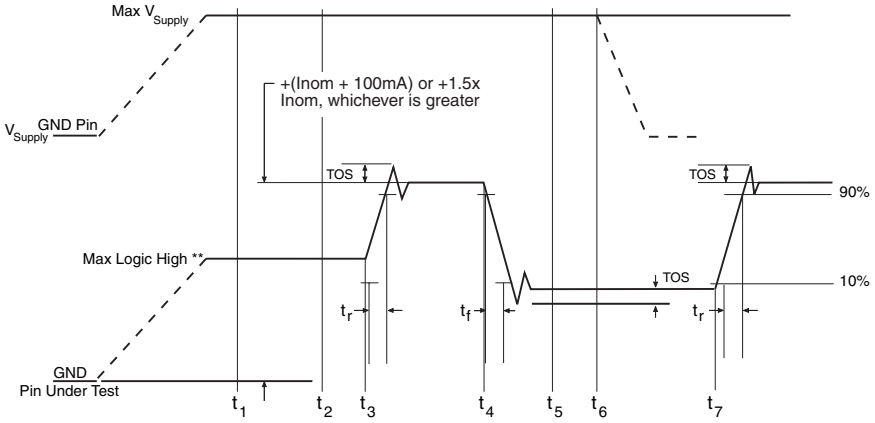
up sensitivity. It should be noted that each lead is curve traced immediately after a current trigger pulse. The lead is skipped if sufficient electrical overstress damage has resulted in an open circuit, short circuit or pin leakage current in excess of the datasheet spec. Testing is performed at a temperature of 85°C.



Time	Operation
T1 → T2	Measure nominal I_{supply} (Inom)
T4 → T7	Cool down time (Tcool)
T4 → T5	Wait time prior to I_{supply} measurement *
T5	Measure I_{supply}
T6	If any $I_{supply} \geq$ the failure criteria defined in section 1.3 (JEDEC 78), latch-up has occurred and power must be removed from DUT

* The wait time shall be sufficient to allow for power supply ramp down and stabilization of I_{supply}.

** Max. logic high and min. logic low shall be per the device specification. When logic levels are used with respect to a nondigital device, min/max voltages (as defined by the device specification) can be supplied to the pin.

Figure 2: Current Trigger Pulse Waveform

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Dielectric Integrity

Time-dependent-dielectric breakdown (TDDB) is one of the principal failure mechanisms in thin dielectric film MOS devices. For this reason, highly reliable, low-defect-density films are essential in the fabrication process. The two types of failure modes associated with dielectric breakdown are:

1. Defect-related breakdown
2. Intrinsic breakdown ("oxide wear-out")

Defect related failures can occur either at low-field or early in the product life. Low-field failures are easily detected by voltage-ramp tests where they fail at much lower than expected voltage levels. That is, they are not able to sustain voltages at operating conditions and would fail instantaneously at these levels. However, some oxides will pass the initial stage but fail early in the product life. Proper screening methods such as burn-in can eliminate these early failures. Defects associated with such failures typically include asperities at the Si-SiO_2 interface, pinholes and microstructural inhomogeneities that affect the barrier height or increase the charge trapping rate. In short, these defects reduce the effective dielectric thickness.

Intrinsic breakdown normally occurs much later in the product life. Because the failure rate associated with this failure mode increases at the end of the reliability life curve, it is sometimes referred to as "oxide wear-out." Charge trapping at the interface and in the oxide is thought to lead to oxide wear-out. At sufficiently high fields, electrons will tunnel through the oxide (Fowler-Nordheim tunneling) towards the anode. Due to impact ionization, some of the high-energy electrons will generate electron-hole pairs in the oxide. Holes will get trapped in the oxide near the Si-SiO_2 interface, increasing the local electric field at the cathode region. More electrons will then tunnel through the region, leading to more impact ionization and, eventually, to a physical rupture of the dielectric film [1].

Accelerated Testing

TDDB failures typically exhibit a Weibull distribution. The fraction of samples that fail at a given time, t, can be approximated by the following equation:

$$F = 1 - e^{-\left(\frac{t_{BD}}{\alpha}\right)^{\beta}} \quad (1)$$

where: F = fraction of test samples that fail

α = time-to-63% failure

ß = Weibull shape factor

t_{BD} = time to breakdown

TDDB performance is found to be a strong function of applied voltage and a weak function of ambient temperature [2]. To practically evaluate TDDB performance of MOS capacitors, accelerated test is done at stress condition, i.e. high voltage and high temperature. Then, TDDB lifetime can be found by extrapolating accelerated test results to use condition, i.e. lower voltage and lower temperature. Operating lifetime or $t(1\%)_O$ is related to accelerated test results according to the following equation:

$$t(1\%)_O = A_{Tot} \times t(1\%)_S \quad (2)$$

where:

$t(1\%)_S$ = time-to-1% failure at stress conditions

$t(1\%)_O$ = time-to-1% failure at operating conditions

V_S = stress voltage

V_O = operating voltage

A_{Tot} = total acceleration factor. It can be written as:

$$A_{Tot} = A_V \times A_T \quad (3)$$

where: A_V = acceleration factor component due to voltage

A_T = acceleration factor component due to temperature

A_V is written as [3]:

$$A_V = e^{\beta_V(\ln V_S - \ln V_O)} \quad (4)$$

where: $ß_V$ = voltage acceleration constant

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It can be obtained experimentally, i.e. from the plot of $(t1\%)_S$ versus applied voltage [3]:

$$\beta_v = \frac{\Delta ln(t1\%)_s}{\Delta ln(V_s)} \quad (5)$$

where:ln(t1%)= natural log of time-to-1% failure

The temperature acceleration factor, A_T, derived from the Arrhenius equation is:

$$A_T = e^{\frac{E_a}{k}\left[\frac{1}{T_o} - \frac{1}{T_s}\right]} \quad (6)$$

where: E_a = activation energy of oxide failure

k = Boltzmann's constant, 8.617×10^{-5}eV/K

T_O = operating temperature (in kelvins)

T_S = stress temperature (in kelvins)

Experimental Procedures

MOS capacitors were evaluated to characterize the integrity of the two gate oxides used in this device. TDDB stress tests were conducted on these structures with varying steady-state dc conditions. A minimum of 29 structures were used for each stress condition. The thicker gate oxide was stressed at 7.400V–8.000V and the thinner gate oxide was stressed at 4.750V–5.125V. All tests were conducted at 100°C. A constant voltage was applied across the dielectric and the time-to-failure monitored. For the thicker oxide, failure was identified when the capacitor under stress ruptured. For the thinner oxide, the generation of current noise during constant voltage stressing was identified as the point of breakdown. This partial breakdown phenomenon is termed as "soft" or "quasi" breakdown [4]. The details on the detection algorithm for such a phenomenon can be found elsewhere [5].

Results

Figure 3 on page 11 and Figure 5 on page 12 show that Weibull distributions were observed for each stress condition when the time-to-failure data was plotted for the thick and thin gate oxides. The $t_{1\%}$ data were extracted from these plots and replotted as a function of the applied dielectric stress. These plots are provided in Figure 4 and Figure 6, respectively. Note that the plots shown are for $t_{1\%}$ data at 100°C. This value represents the maximum internal Si junction temperature in a 70°C external environment. The lifetimes of the gate oxides were extracted from Figure 4 and Figure 6. Under maximum operating conditions, the lifetimes were found to be in excess of 10 years.

References

1. I.C. Chen, S. Holland and C. Hu, "Hole Trapping and Breakdown in Thin SiO2," *IEEE Electron Device Letters*, Vol. EDL-7, 1986 p. 164.

2. J.W. McPherson, D.A. Baglee, "Acceleration Factors for Thin Gate Oxide Stressing," *IEEE International Reliability Physics Symposium*, 1985, p.1.

3. E. Y. Wu et al., "CMOS Scaling Beyond the 100-nm Node with Silicon-Dioxide-Based Gate Dielectrics," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, p. 287.

4. M. Depas, T. Nigam, M.M. Heyns, "Soft Breakdown of Ultra Thin Gate Oxides," *IEEE Trans. on Electron Devices*, Vol. 43, 1996, p. 1499.

5. P. Roussel, R. Degraeve, G. Van den Bosch, B. Kaczer, G. Groeseneken, "Accurate and Robust Noise-Based Trigger Algorithm for Soft Breakdown Detection in Ultra Thin Oxides," *IEEE International Reliability Physics Symposium*, 2001, p. 386.

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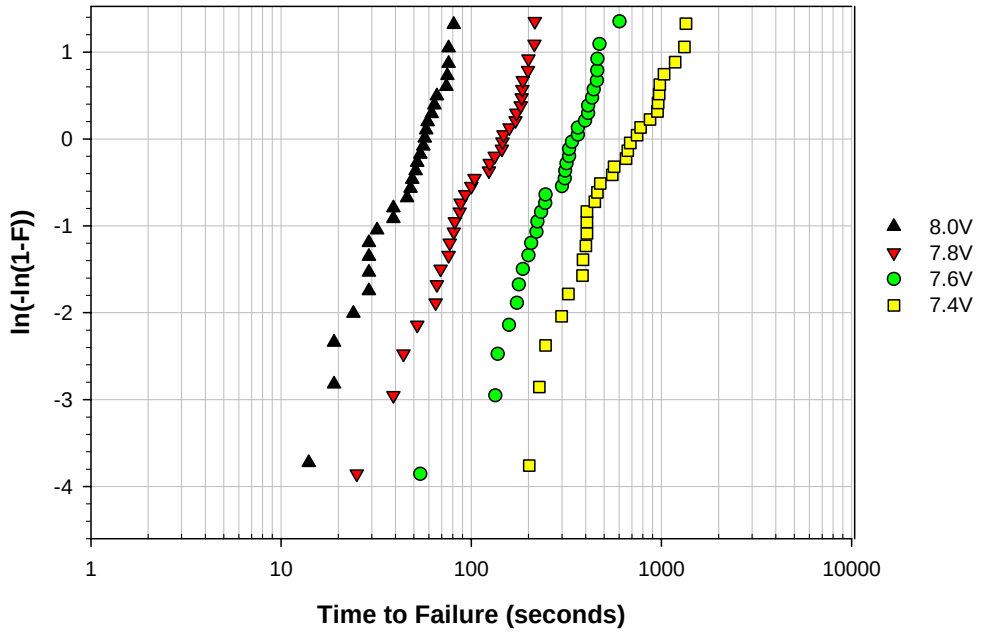

Figure 3: Weibull Distribution of Failure Times at Various Stress Levels (Thick Gate Oxide)

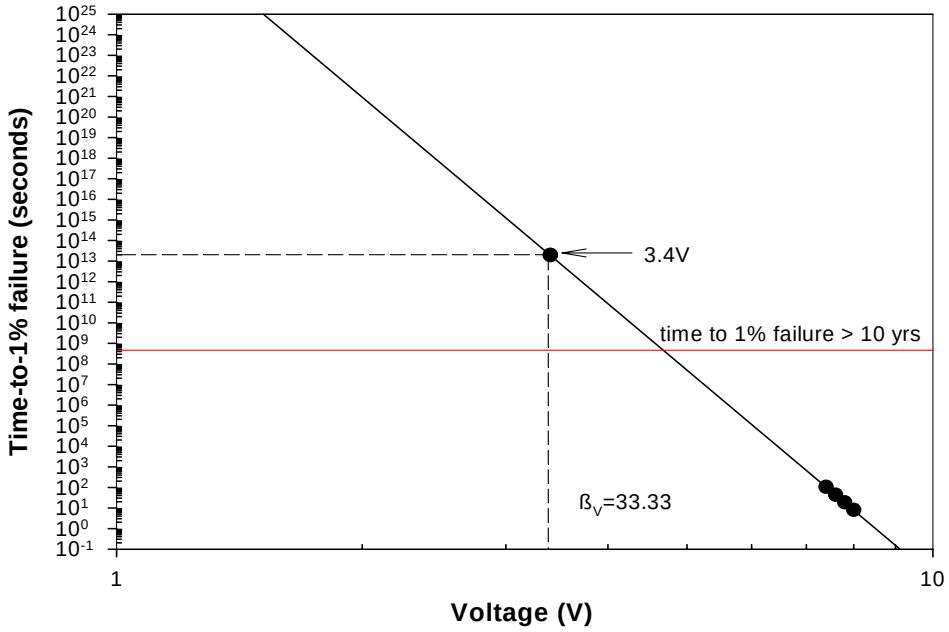

Figure 4: Time to 1% Failure as a Function of Stress Voltage (Thick Gate Oxide)

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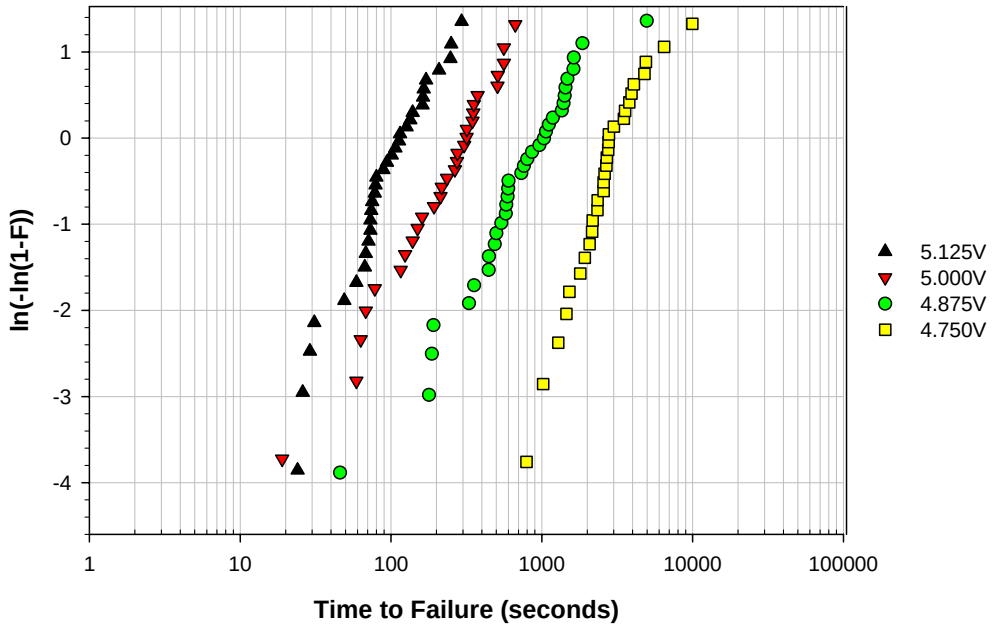

Figure 5: Weibull Distribution of Failure Times at Various Stress Levels (Thin Gate Oxide)

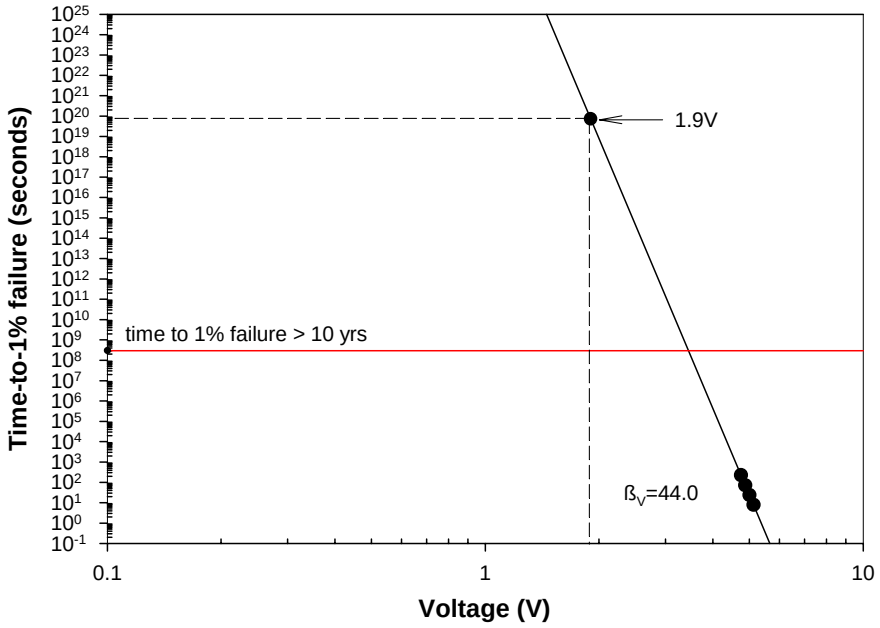

Figure 6: Time to 1% Failure as a Function of Stress Voltage (Thin Gate Oxide)

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Electromigration

As metal-line cross sections continue to shrink, electromigration has become a primary reliability concern in thin conducting films. The long-term reliability of narrow interconnects is severely limited by this phenomenon. Electromigration-induced failures under an applied current stress are due to a mass-flux divergence caused by inhomogeneities in the microstructure and temperature gradients. A nonuniform mass transport caused by the interaction between metal atoms and a direct current results in depletion and accumulation of metal atoms. That is, when a high current flows through the conductor, diffusion of the metal ions is in the direction of electron flow. The net atomic flux or mass flow, J_A, is given by the Huntington relationship [1]:

$$J_A = \frac{N}{kT} Z^* e \rho j D_0 e^{\left[\frac{-E_a}{kT}\right]} \quad (1)$$

where: N = density of ions

D_0 = self-diffusion constant

E_a = activation energy

k = Boltzmann's constant

T = absolute temperature

Z*e = effective charge on the migrating ion

ρ = resistivity of the film

j = current density

At a positive flux divergence, where more material enters a region than leaves it, an accumulation of metal ions occurs, resulting in extrusions or shorts. Where more material leaves a region than enters it, negative flux divergence exists, causing mass depletion, which results in voids or opens.

Acceleration Testing

To evaluate the long-term reliability of thin conduction films, accelerated testing [2,3] is typically conducted on test structures with minimum dimensions. The stressing of test structures is achieved through constant high-current densities and elevated temperatures. Each device under stress is monitored for failure due to electromigration and the time-to-failure recorded. The measured lifetime values at the accelerated levels are then extrapolated to use conditions. To relate the median time-to-failure of thin film conductors to current density and temperature, Black [4] proposes the following model:

$$MTF = \left[\frac{A}{J^n}\right] e^{\left[\frac{E_a}{kT}\right]} \quad (2)$$

where: A = parameter depending on geometry, physical characteristics of film and substrate, and protective overcoating

J = current density

n = constant (~2.0)

E_a = activation energy (varies for different metal compositions)

k = Boltzmann's constant

T = absolute temperature

From the above equation, the current acceleration factor is:

$$\frac{MTF_o}{MTF_s} = \left[\frac{J_s}{J_o}\right]^n \quad (3)$$

and the temperature acceleration factor is:

$$\frac{MTF_o}{MTF_s} = e^{\frac{E_a}{k}\left[\frac{1}{T_o} - \frac{1}{T_s}\right]} \quad (4)$$

where: MTF_o = median time-to-failure at operating condition

MTF_s = median time-to-failure at stress condition

J_o = operating current density

J_s = stress current density

T_o = operating temperature (in kelvins)

T_s = stress temperature (in kelvins)

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All new metallization technologies are characterized by accelerated stress tests, as described above, to ensure that the specified design rules meet the failure rate goals. The minimum time-to-failure criterion is set so that no electromigration failures are induced within a 10-year period at operating conditions.

Test Procedures and Results

To determine the long-term reliability of the metal process, a conventional electromigration test was performed. This test is conducted at elevated temperatures and dc currents in order to accelerate metal-line failures. The stress conditions used are high enough to precipitate the failure mechanism, yet not so high as to cause failures unrelated to the metal reliability or make extrapolation from stress conditions to maximum use conditions difficult.

For this evaluation a minimum dimension via structure was used. These structures were bonded and packaged in 20-lead ceramic DIP packages. Tests were conducted on 32 sample devices. The stress current for this structure was 9.4mA and the stress temperature was 190°C. The failure criteria was an open.

Extrapolating to maximum use conditions (100°C, 4mA/μm^2) using Black's equation with an activation energy of 0.7eV and n=2, the minimum lifetime of the metal process is greater than 10 years. Data from a via chain electromigration failure distribution is provided in the below figure.

References

1. H.B. Huntington and A.R. Grone, "Current-Induced Marker Motion in Gold Wires," *The Journal of Physics and Chemistry of Solids*, Vol. 20, 1961, p. 76.

2. JEDEC Standard JESD63, *Standard Method for Calculating the Electromigration Model Parameters for Current Density and Temperature*, 1998.

3. JEDEC Standard JESD33, *Standard Method for Measuring and Using the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line*, 1995.

4. J.R. Black, "Electromigration – A Brief Survey and Some Recent Results," *IEEE Transactions on Electron Devices*, Vol. ED-16, 1969, p. 338.

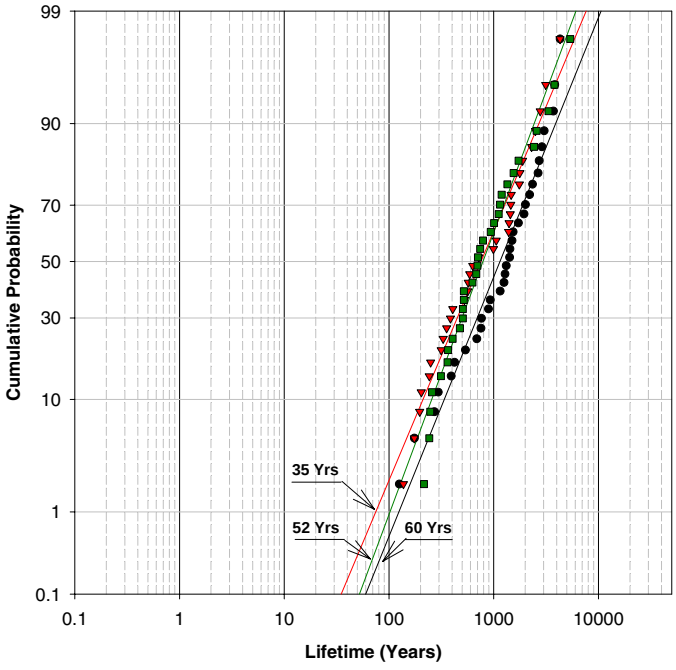

Figure 7: Via Electromigration Log Normal Plot

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Array Configuration

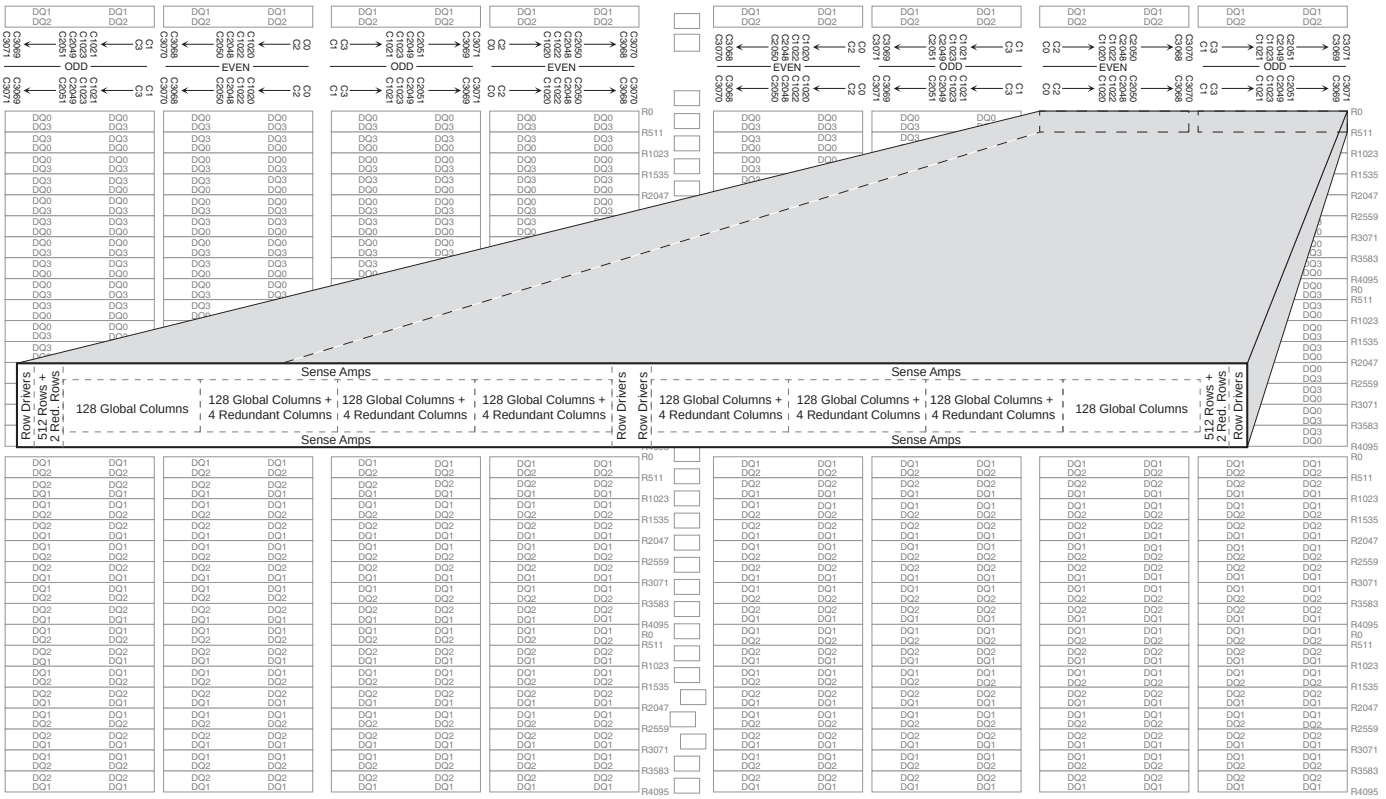

Figure 8: Array Configuration — 128 Meg × 4 — Zoomed-in View, Bank 2

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Array Configuration (continued)

Figure 9: Array Configuration — 128 Meg × 4

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Array Configuration (continued)

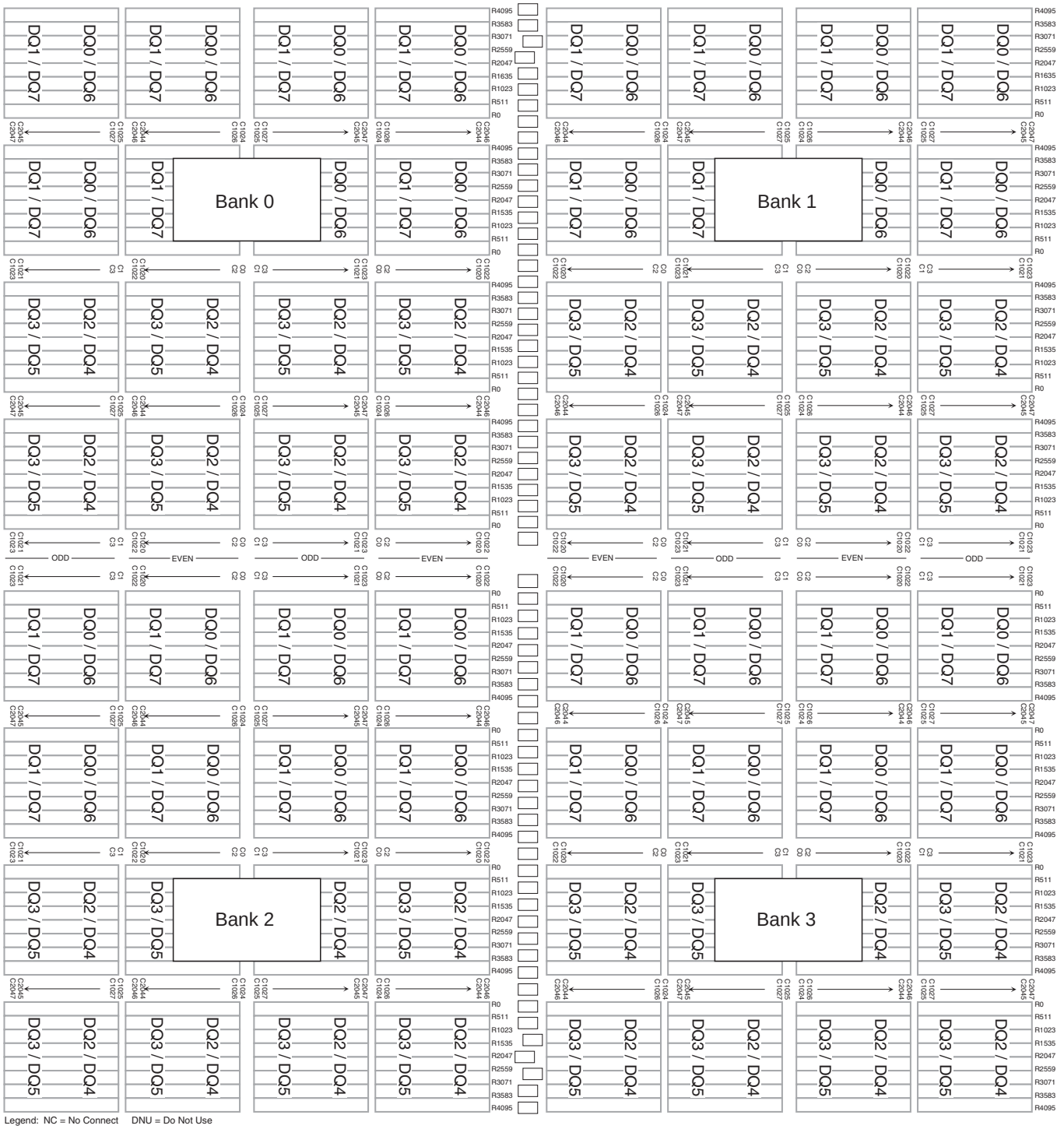

Figure 10: Array Configuration — 64 Meg × 8

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Array Configuration (continued)

Figure 11: Array Configuration — 32 Meg × 16

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Address Topological Diagram

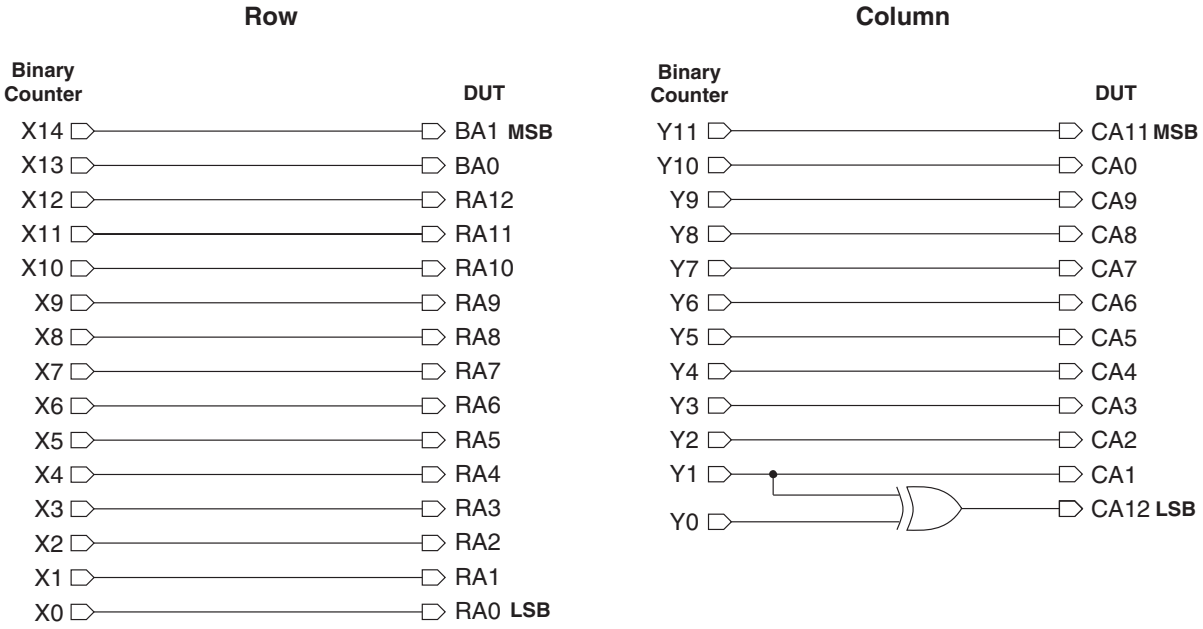

Figure 12: Address Topological Diagram — 128 Meg × 4

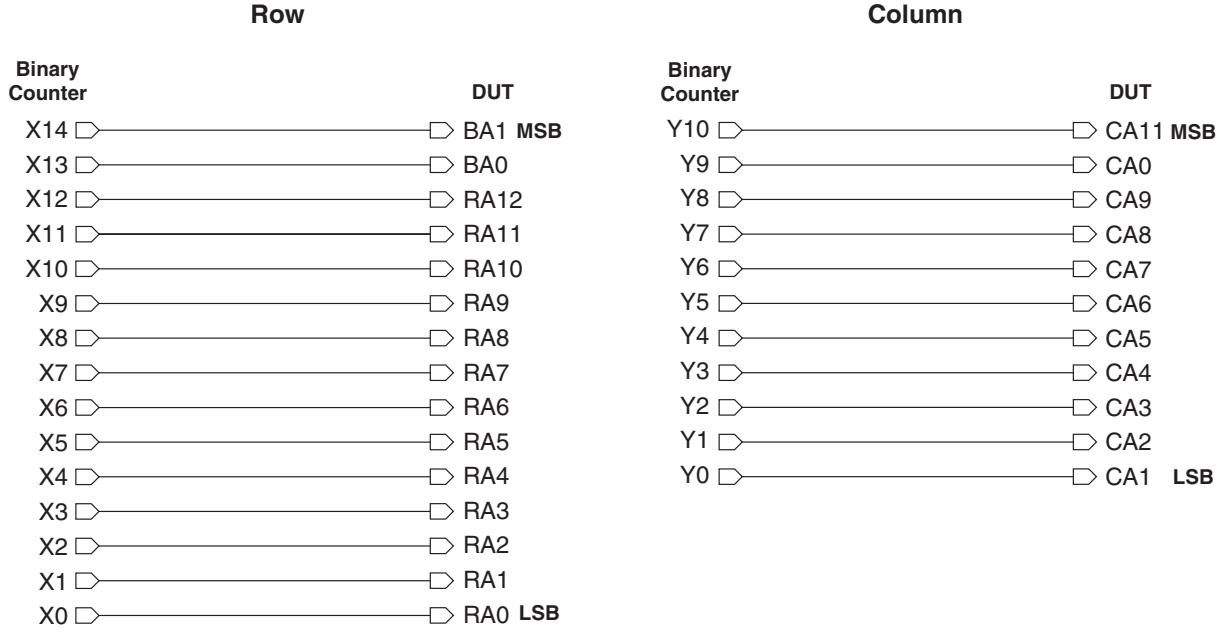

Figure 13: Address Topological Diagram — 64 Meg × 8

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Address Topological Diagram (continued)

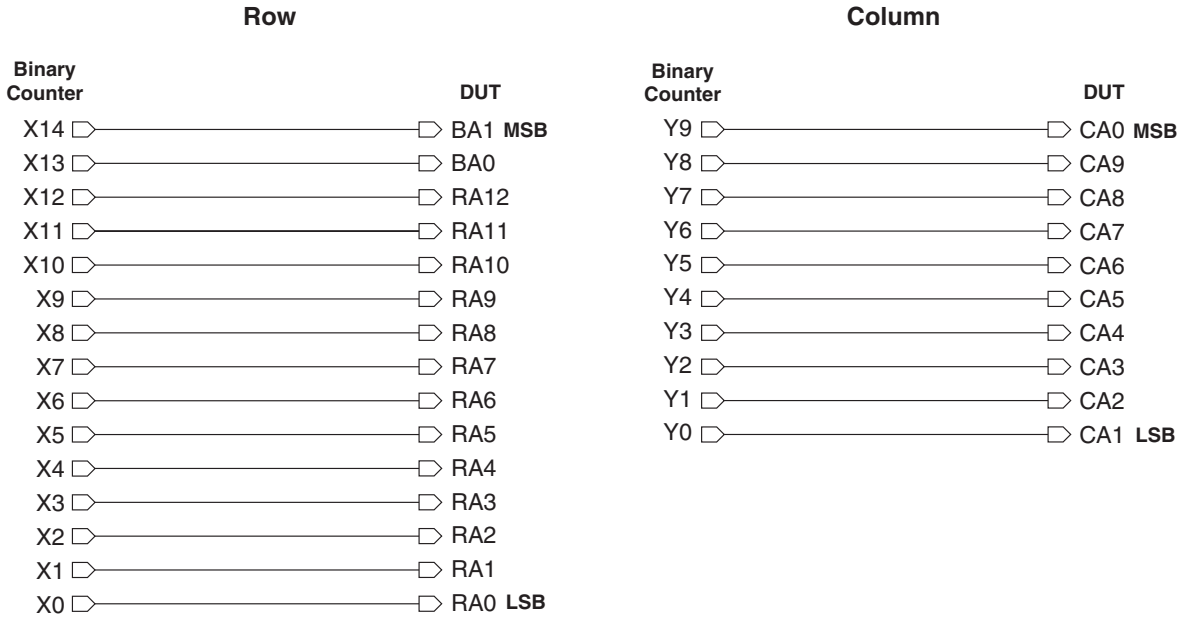

Figure 14: Address Topological Diagram — 32 Meg × 16

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Karnaugh Maps

128 Meg x 4	DQs 0 through 3
64 Meg x 8	DQs 0 through 7
32 Meg x 16	DQs 0 through 15

DUT Address

RA0	RA1	
0	0	T
0	1	C
1	0	C
1	1	T

Counter Address

X0	X1	
0	0	T
0	1	C
1	0	C
1	1	T

T = True Data: A cell is charged to V_{DD} when the DQ is logic "1."
C = Complement Data: A cell is charged to V_{DD} when the DQ pin is logic "0."

Figure 15: Karnaugh Maps

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Data Topology Equations

For Solids Ones Background:

128 Meg x 4	DQs 0 through 3	RA0 ⊕ RA1
64 Meg x 8	DQs 0 through 7	
32 Meg x 16	DQs 0 through 15	

Figure 16: Data Topology Equations

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Address Topology

		MSB														LSB
		BA1	BA0	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
Row	0	x	x	0	0	0	0	0	0	0	0	0	0	0	0	0
Row	1	x	x	0	0	0	0	0	0	0	0	0	0	0	0	1
Row	2	x	x	0	0	0	0	0	0	0	0	0	0	0	1	0
Row	3	x	x	0	0	0	0	0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	Binary Up Count		.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
Row	2046	x	x	0	0	1	1	1	1	1	1	1	1	1	1	0
Row	2047	x	x	0	0	1	1	1	1	1	1	1	1	1	1	1
Row	2048	x	x	0	1	0	0	0	0	0	0	0	0	0	0	0
Row	2049	x	x	0	1	0	0	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	Binary Up Count		.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
Row	4094	x	x	0	1	1	1	1	1	1	1	1	1	1	1	0
Row	4095	x	x	0	1	1	1	1	1	1	1	1	1	1	1	1
Row	4096	x	x	1	0	0	0	0	0	0	0	0	0	0	0	0
Row	4097	x	x	1	0	0	0	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	Binary Up Count		.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
Row	6142	x	x	1	0	1	1	1	1	1	1	1	1	1	1	0
Row	6143	x	x	1	0	1	1	1	1	1	1	1	1	1	1	1
Row	6144	x	x	1	1	0	0	0	0	0	0	0	0	0	0	0
Row	6145	x	x	1	1	0	0	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	Binary Up Count		.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
Row	8190	x	x	1	1	1	1	1	1	1	1	1	1	1	1	0
Row	8191	x	x	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: Row topology is identical for all 4 banks (i.e., Bank0, Bank1, Bank2, Bank3). BA1 and BA0 determine which bank is selected. The following table identifies which bank is being addressed based upon the values of BA1 and BA0.

Bank	BA1	BA0
0	0	0
1	0	1
2	1	0
3	1	1

Figure 17: Row Address Topology — 128 Meg × 4, 64 Meg × 8 and 32 Meg × 16

Address Topology (continued)

Column Topology — 128 Meg x 4

Column		MSB CA11	CA0	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	LSB CA12
Column	0	0	0	0	0	0	0	0	0	0	0	0	0
Column	1	0	0	0	0	0	0	0	0	0	0	0	1
Column	2	0	0	0	0	0	0	0	0	0	0	1	1
Column	3	0	0	0	0	0	0	0	0	0	0	1	0
Column	4	0	0	0	0	0	0	0	0	0	1	1	0
Column	5	0	0	0	0	0	0	0	0	0	1	1	1
Column	6	0	0	0	0	0	0	0	0	0	1	0	1
Column	7	0	0	0	0	0	0	0	0	0	1	0	0
Column	8	0	0	0	0	0	0	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	Binary Up Count		.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.
Column	2040	0	1	1	1	1	1	1	1	1	0	1	0
Column	2041	0	1	1	1	1	1	1	1	1	0	1	1
Column	2042	0	1	1	1	1	1	1	1	1	0	0	1
Column	2043	0	1	1	1	1	1	1	1	1	0	0	0
Column	2044	0	1	1	1	1	1	1	1	1	1	0	0
Column	2045	0	1	1	1	1	1	1	1	1	1	0	1
Column	2046	0	1	1	1	1	1	1	1	1	1	1	1
Column	2047	0	1	1	1	1	1	1	1	1	1	1	0
Column	2048	1	0	0	0	0	0	0	0	0	0	0	0
Column	2049	1	0	0	0	0	0	0	0	0	0	0	1
Column	2050	1	0	0	0	0	0	0	0	0	0	1	1
Column	2051	1	0	0	0	0	0	0	0	0	0	1	0
Column	2052	1	0	0	0	0	0	0	0	0	1	1	0
Column	2053	1	0	0	0	0	0	0	0	0	1	1	1
Column	2054	1	0	0	0	0	0	0	0	0	1	0	1
Column	2055	1	0	0	0	0	0	0	0	0	1	0	0
Column	2056	1	0	0	0	0	0	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	Binary Up Count		.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.
Column	4088	1	1	1	1	1	1	1	1	1	0	1	0
Column	4089	1	1	1	1	1	1	1	1	1	0	1	1
Column	4090	1	1	1	1	1	1	1	1	1	0	0	1
Column	4091	1	1	1	1	1	1	1	1	1	0	0	0
Column	4092	1	1	1	1	1	1	1	1	1	1	0	0
Column	4093	1	1	1	1	1	1	1	1	1	1	0	1
Column	4094	1	1	1	1	1	1	1	1	1	1	1	1
Column	4095	1	1	1	1	1	1	1	1	1	1	1	0

Figure 18: Column Address Topology — 128 Meg × 4

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Address Topology (continued)

Column Topology — 64 Meg x 8

Column		MSB CA11	CA0	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	LSB CA1
Column	0	0	0	0	0	0	0	0	0	0	0	0
Column	1	0	0	0	0	0	0	0	0	0	0	1
Column	2	0	0	0	0	0	0	0	0	0	1	0
Column	3	0	0	0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	Binary Up Count		.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	.	.	
Column	1020	0	1	1	1	1	1	1	1	1	0	0
Column	1021	0	1	1	1	1	1	1	1	1	0	1
Column	1022	0	1	1	1	1	1	1	1	1	1	0
Column	1023	0	1	1	1	1	1	1	1	1	1	1
Column	1024	1	0	0	0	0	0	0	0	0	0	0
Column	1025	1	0	0	0	0	0	0	0	0	0	1
Column	1026	1	0	0	0	0	0	0	0	0	1	0
Column	1027	1	0	0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	Binary Up Count		.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	.	.	
Column	2044	1	1	1	1	1	1	1	1	1	0	0
Column	2045	1	1	1	1	1	1	1	1	1	0	1
Column	2046	1	1	1	1	1	1	1	1	1	1	0
Column	2047	1	1	1	1	1	1	1	1	1	1	1

Figure 19: Column Address Topology — 64 Meg × 8

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Address Topology (continued)

Column		MSB CA0	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	LSB CA1
Column	0	0	0	0	0	0	0	0	0	0	0
Column	1	0	0	0	0	0	0	0	0	0	1
Column	2	0	0	0	0	0	0	0	0	1	0
Column	3	0	0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	Binary Up Count		.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
Column	508	0	1	1	1	1	1	1	1	0	0
Column	509	0	1	1	1	1	1	1	1	0	1
Column	510	0	1	1	1	1	1	1	1	1	0
Column	511	0	1	1	1	1	1	1	1	1	1
Column	512	1	0	0	0	0	0	0	0	0	0
Column	513	1	0	0	0	0	0	0	0	0	1
Column	514	1	0	0	0	0	0	0	0	1	0
Column	515	1	0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	Binary Up Count		.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
Column	1020	1	1	1	1	1	1	1	1	0	0
Column	1021	1	1	1	1	1	1	1	1	0	1
Column	1022	1	1	1	1	1	1	1	1	1	0
Column	1023	1	1	1	1	1	1	1	1	1	1

Figure 20: Column Address Topology — 32 Meg × 16

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Memory Cell Definition

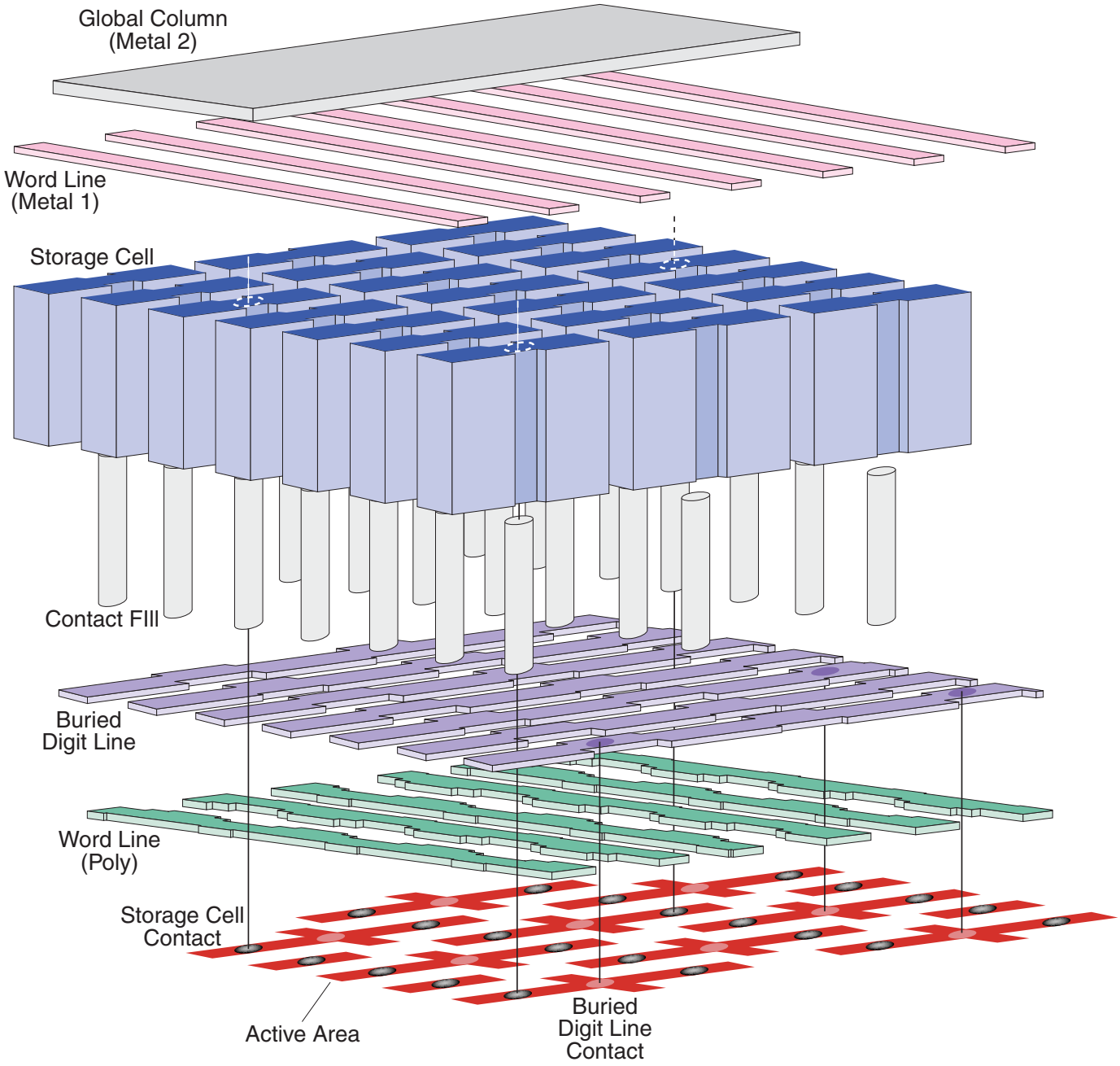

Figure 21: Memory Cell Definition — Exploded View

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Memory Cell Definition (continued)

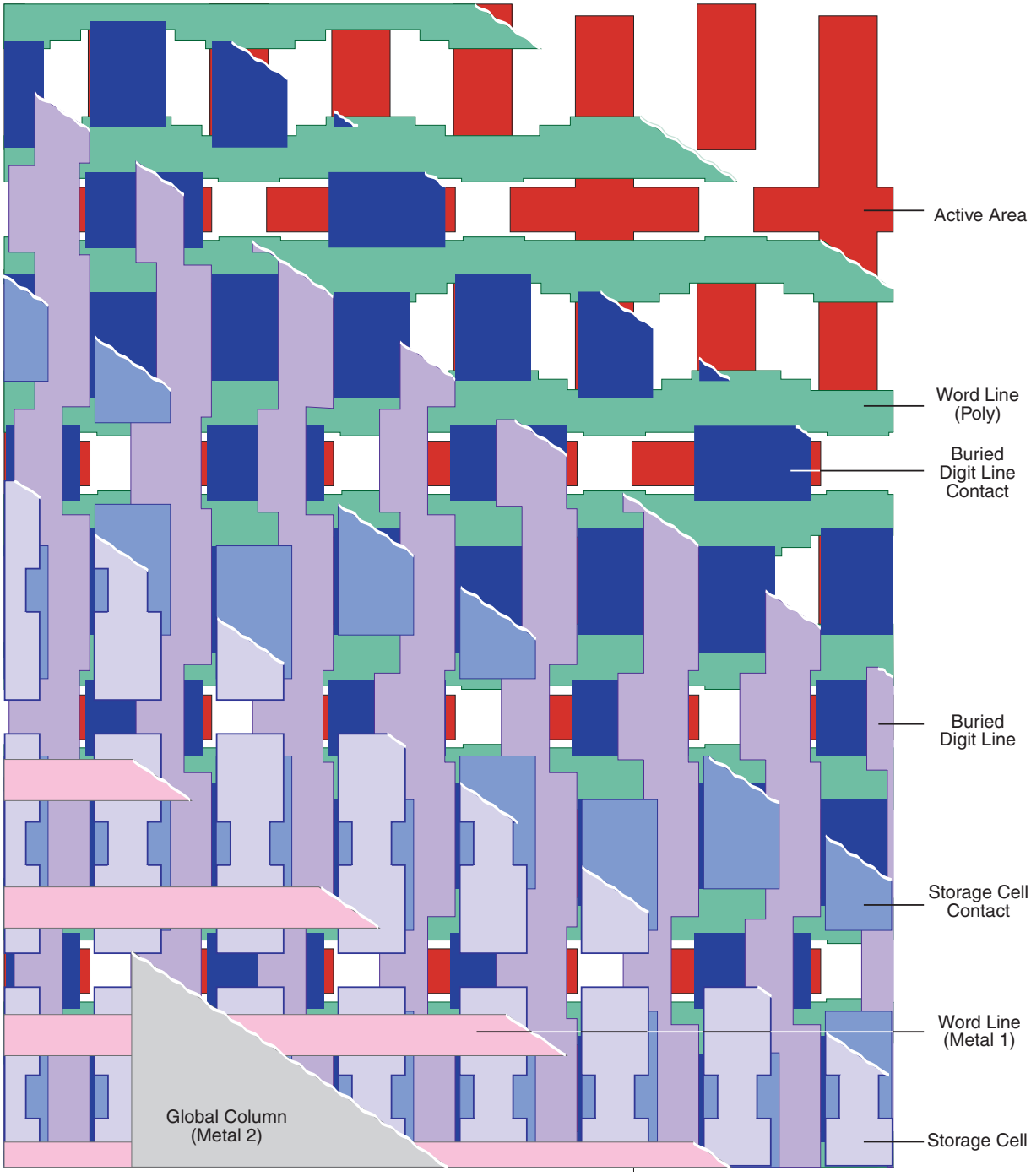

Figure 22: Memory Cell Definition — Top-Down View

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Memory Cell Definition (continued)

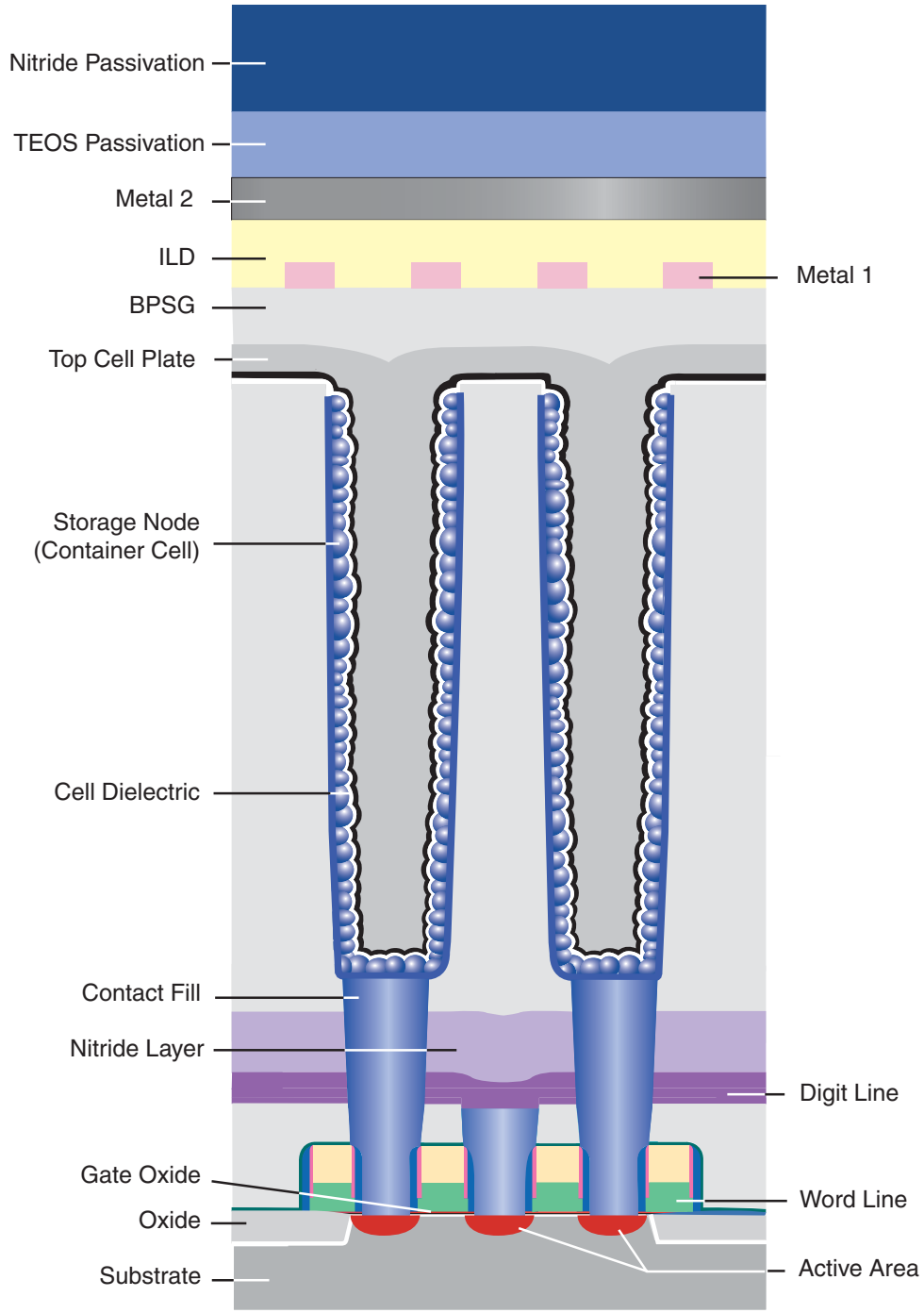

Figure 23: Memory Cell Definition — Cross Section View

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Thermal Impedance

Overview

Thermal impedance parameters are used to describe the rate at which a package dissipates heat in the JEDEC environment. These values are used to compare the thermal performance of various packages. θ_{JA} is a measurement of the thermal resistance between the junction of the device under test and the surrounding environment. A wind tunnel provides a controlled moving air environment, in which parts are tested at 1m/s and 2m/s. When measured/modeled in a moving-air environment, the resistance is identified as θ_{JMA}. θ_{JC} is a measurement of the junction-to-case thermal resistance and is measured/modeled with the top of the part attached to an isothermal copper block. For this measurement the part is not attached to a test board. The wires are soldered directly to the leads and the device is held in place with thermal grease. This method does not conform to JEDEC standards, as JEDEC does not have a procedure for measuring θ_{JC}. θ_{JB} is a measurement of the junction-to-board thermal resistance. For this measurement, heat generated by the device is forced from the device to the board via isothermal copper blocks. During this process the other surfaces are insulated to ensure that only power flowing between the device and the board is measured/modeled. θ_{JA}, $\theta_{JMA,}$ and θ_{JB} measurements are taken with the IC package surface-mounted to a PCB that has been designed to JEDEC standards. JEDEC defines two different test boards: a high-conductive 4-layer and low conductive 2-layer test board. If measured, the data provided in the following table represents measurements taken on six samples.

It should be emphasized that these parameters are provided solely for the purpose of comparing device/package combinations and should not be used for junction temperature predictions.†

Table 10: Summary of Thermal Impedance

Die Size (Sq mm)	Package	Number of Leads	Test Board	θ_{JA} (°C/Watt) 0m/s	θ_{JMA} (°C/Watt) 1m/s	θ_{JMA} (°C/Watt) 2m/s	θ_{JB} (°C/Watt)	θ_{JC} (°C/Watt)
94.00	TSOP	54	2-Layer	62.6	48.4	44.2	19.2	6.7
			4-Layer	39.2	32.3	30.6	19.3	

Test Method Summary

Alliance Memory follows JEDEC standard JESD51 test methods and procedures for measuring or modeling thermal resistance. The thermal resistance between the junction (J) of the device and some other point (X) is calculated using the following equation, where θ_{JX} is the thermal resistance between these two points. When calculating the thermal resistance between the junction and a specific location, such as the board (B), the thermal resistance would be expressed as θ_{JB}.

$$\theta_{JX} = (T_J - T_X)/P_H$$

where: θ_{JX} = thermal resistance between the junction of the device and some other location (°C/Watt)

T_J = temperature of the junction (°C)

T_X = temperature of the location for which thermal resistance is being measured (°C)

P_H = power applied to the device producing an increase in junction temperature (W)

† For junction temperature predictions, finite element analysis (FEA) or computational fluid dynamics (CFD) modeling should be used.

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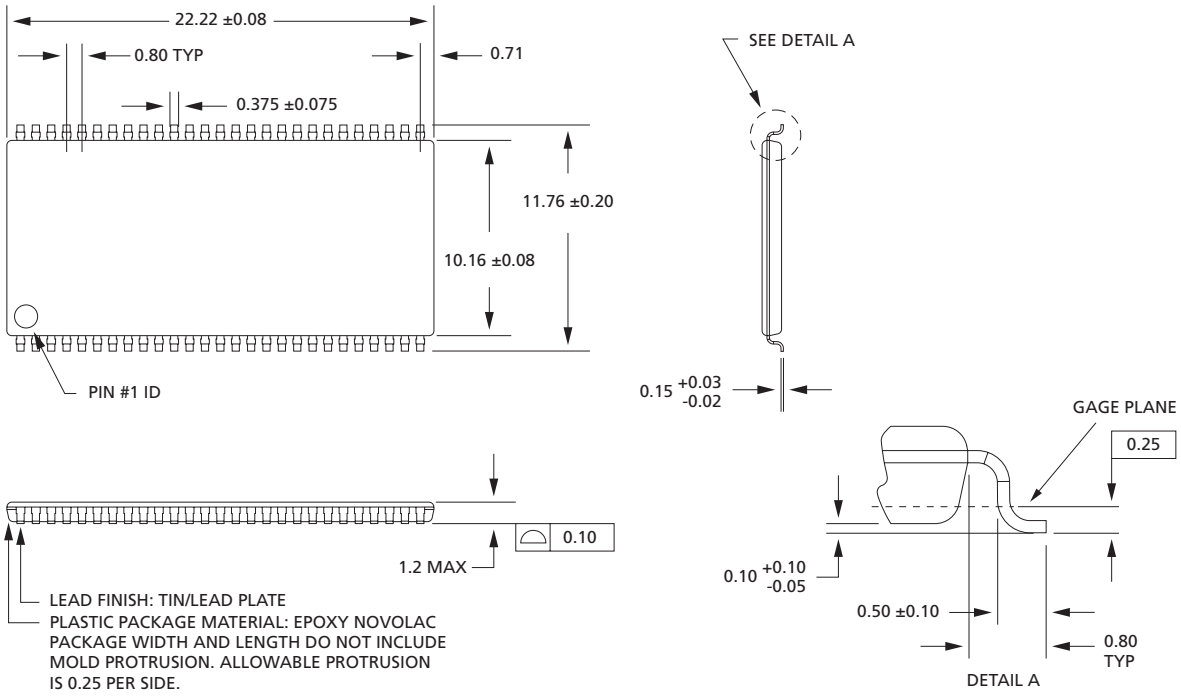
Typical Package Characteristics



Notes:
1) All dimensions in millimeters.
2) Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

Figure 24: Package Illustration — 54L TSOP

Table 11: Interposer/Package Characteristics — TSOP

Plating Finish	90Sn10Pb or pure matte Sn	
Interposer Material	42Ni57Fe (less than 1% other)	
CTEs	Mold compound:	6–15 ppm/°C
	Interposers:	4.2–4.7 ppm/°C
Flammability Rating	Interposer Laminate:	50-80 LOI
	Mold Compound:	28-40 LOI
	Limited Oxygen Index determined by test method JIS K 7201 or ASTM D2863.	

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Input/Output Capacitance

Equipment: HP8753ES VNA Meter.

Conditions: I/O capacitance testing for Alliance Memory's 512Mb SDRAM (TSOP package) was conducted at ambient temperature, 3.3V V_{DD}/V_{DDQ}, 1.4V bias, 100Mhz.

Measurements demonstrated compliance with Alliance Memory's data sheet specifications, as provided in the table below.

Table 12: Input/Output Capacitance

Parameter	Min (pF)	Max (pF)
Input capacitance: CLK	2.5	3.5
Input capacitance: All other input-only pins	2.5	3.8
Input/Output capacitance: DQs	4.0	6.0

Moisture Sensitivity Level

Sample Size: A minimum of 3 lots are used for each MSL evaluated.

Preconditioning: Devices are baked for a minimum of 8 hours at 125°C.

Test Conditions: Soak conditions for moisture sensitivity levels defined in IPC/JEDEC standard J-STD-020:

Level 1 – 168 hours at 85°C and 85%RH
Level 2 – 168 hours at 85°C and 60%RH
Level 3 – 192 hours at 30°C and 60%RH
Level 4 – 96 hours at 30°C and 60%RH
Level 5 – 72 hours at 30°C and 60%RH
Level 5a – 48 hours at 30°C and 60%RH

Following soak, the devices are run 3 times through a convection reflow oven, reaching a peak temperature of 260°C. The devices are then evaluated using visual, electrical and C-SAM analysis.

Table 13: Moisture Sensitivity Level Test Results

Package	MSL	Failed/Tested
54L TSOP	Level 4	0 / 30

The floor life (out of bag) for product stored at ≤30°C/60%R.H. is defined by IPC/JEDEC standard J-STD-020 as noted below:

Level 1 = unlimited at ≤30°C/85%R.H.	Level 3 = 168 Hours	Level 5 = 48 Hours
Level 2 = 1 year	Level 4 = 72 Hours	Level 5a = 24 Hours

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Solderability

Sample Size: A minimum of 3 lots are used for this test.

Preconditioning: Samples are steam-aged at 91°C, -5°/+3°C for 8 hours.

Test Conditions: Samples are surface mounted onto an FR4 substrate with low activity (LO) SnPb solder paste and run through a convection reflow oven reaching a peak temperature of 215°C. Following the test, samples are visually inspected for acceptable wetting.

Alliance Memory references J-STD-002 when conducting Solderability testing.

Table 14: Solderability Test Results

Package	Failed / Tested
54L TSOP	0 / 15

Bond Integrity

Sample Size: A minimum of 3 lots are used for each test.

Preconditioning: Samples are baked at 165°C for 72 hours.

Alliance Memory references JEDEC standard JESD22-B116 when conducting Wire Bond Shear testing and follows internal Alliance Memory specifications when conducting Wire Pull testing.

Table 15: Bond Integrity Test Results

Package	Wire Bond Shear			Wire Pull		
	Sample Size	Min. (gmf)	Mean (gmf)	Sample Size	Min. (gmf)	Mean (gmf)
54L TSOP	513	23.8	29.7	513	6.0	7.5

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Fabrication Process Steps

INCOMING MATERIAL All starting material is verified for cleanliness, uniformity and compliance with Alliance Memory specifications. Each silicon wafer receives a unique laser scribe for total product traceability.

PHOTOLITHOGRAPHY Wafers are coated with a layer of light-sensitive photoresist. Specified sections of the wafer are exposed by projecting ultraviolet light onto the wafer through a mask. A photoresist pattern, which will protect an underlying film from a subsequent etch step, is produced.

ETCH The areas of the wafer not protected by the exposed photoresist are removed by either plasma (dry etch) or acid (wet etch). The result is the definition of a given feature(s), such as a hole or line. The photoresist is then cleaned or "stripped" off the wafer, leaving a pattern in the exact design of the mask.

IMPLANT Wafers are bombarded with positively or negatively charged dopant ions, which are implanted into the silicon. This process, called "doping," changes the electrical characteristics in selected areas of the silicon and forms conductive regions on the wafer.

DIFFUSION Silicon dioxide, nitride and polysilicon layers are formed on the wafer during a number of high-temperature furnace processes. The wafers are exposed to various gases, which either react with the silicon, causing it to oxidize and form an SiO_2 layer, or react with each other to form poly and nitride deposits. These layers are patterned using photolithography and form the layers of the diodes, transistors, and capacitors of the circuit. High-temperature furnaces are also used to introduce and diffuse dopants into the wafers.

METAL A thin layer of aluminum or other metal is deposited and patterned, forming interconnections between various regions of the die.

PASSIVATION The fabrication process is completed by depositing a final glass layer on the wafer. This layer protects the circuits from contamination or damage during the testing and packaging process flows.

PROBE When the fabrication process is complete, each wafer consists of many discrete integrated circuits or "die." Each die on the wafer is electrically tested using tiny probes that connect the metalized pads on the die to the test station computer. This probe testing produces wafer maps that store data on each functioning die. The wafer maps are used later during the assembly process to ensure that only good die are packaged.

TO ASSEMBLY Assembly (see next page).

Figure 25: Fabrication Process Steps

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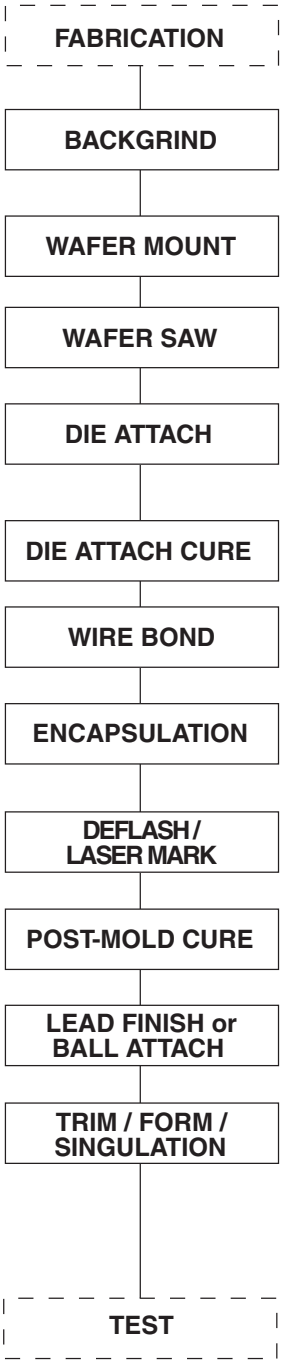
Assembly Process Flow



The fabrication process yields silicon wafers containing many discrete integrated circuits or dice. Following fabrication, the wafers undergo assembly processing where the individual dice are separated and encapsulated according to package specifications.

Wafers are ground to the desired thickness using in-feed wafer grinding equipment. Tape is applied to the front side of the wafer for protection during backgrind and is removed when the grinding process has been completed.

Fabricated wafers are automatically mounted on a carrying film.

The individual dice on the wafer are then separated using a high-speed diamond-blade saw and high water pressure. The carrying film holding the die remains undisturbed by the saw.

Using automated pick-and-place equipment, the good dice (identified by the probe-generated wafer map) are removed from the carrier film. With the aid of a special double-sided adhesive tape or epoxy, each die is attached to the interposer.

To fully polymerize the die attach media, the die-attached interposers are cured.

Using high-speed automated equipment, the aluminum circuits on the die are connected to the appropriate leads with gold wire.

Interposers (with dice and interconnections) are placed in heated mold cavities. Using a hydraulic mechanism, hot thermosetting plastic is transferred into the cavities, forming encapsulated devices.

Prior to lead-finish processing, the leaded devices are run through chemical baths to clean lead surfaces. This process is known as deflash. A laser mark, providing traceability to the assembly manufacturing lot, is scribed on the package.

Molded interposers are placed in an oven to complete the polymerization of the epoxy encapsulant.

If the product has leads, the leads of each device receive a finish of tin/lead electroplating to ensure reliable application by the customer. If the product has solder balls, the balls are placed and attached using a reflow process.

A press-and-tool set is used to cut the interposers, separating the encapsulated dice into discrete devices, and forming the leads into appropriate shape for the package specified.

Product is electrically tested to screen out assembly related failures. Parametric tests detect open connections, shorts, and severe leakage. A basic functionality test is performed to assure proper pin operation.

Test (see next page).

Figure 26: Assembly Process Flow

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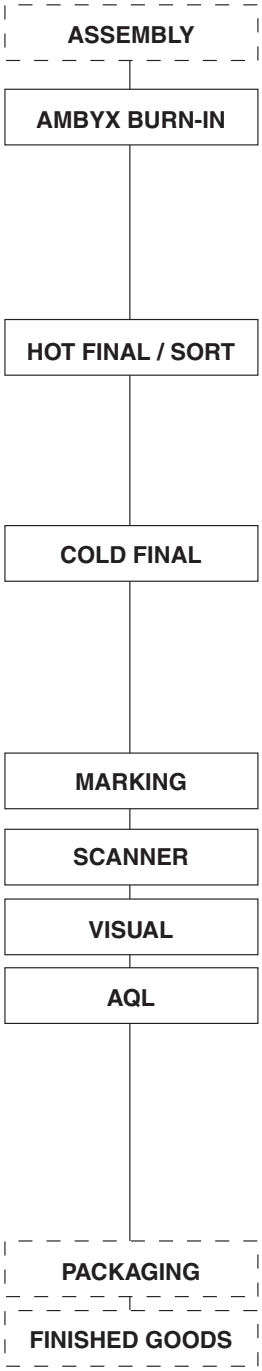
Test Process Flow — Packaged Parts



During the assembly process, the discrete integrated circuits (fabricated on the silicon wafers during fabrication processing) are separated into individual dice and packaged.

Alliance Memory uses its exclusive AMBYX intelligent burn-in and test system to screen out infant mortalities and perform functional pattern tests at ambient, cold and hot temperatures. Devices are dynamically burned-in for a specified duration using multiple patterns at 125˚C and high VDD. Devices are also functionally tested every hour at burn-in conditions (125˚C) to verify that the devices under test are being properly exercised. The functional pattern tests consist of low/high VDD margin, dynamic (distributed only) and static refresh, as well as a wide range of additional algorithms and data backgrounds at temperatures above the maximum and below the minimum specified in the data sheet. Testing is performed while temperatures are being ramped to ensure wirebond integrity and to screen for thermal intermittent opens.

All testing (including speed sorting, parametric and functional testing) is conducted above the maximum datasheet specified temperature. Parametric tests are performed to detect opens, shorts, input/output leakage and to determine whether input/output voltage levels, and standby and operating currents are within specified limits. Functional tests include low/high VDD margin, VDD bump, low/high VDD speed verification, dynamic (distributed and disturbed) and static refresh, as well as a full range of array exercising algorithms. These algorithms are run with guardbanded voltage levels and timing parameters with varied data backgrounds to verify AC parameters and to identify any timing, voltage, or pattern sensitive defects.

Parametric and functional tests are conducted below the minimum datasheet specified temperature. Parametric tests are performed to detect opens, shorts, and input/output leakage, and to determine whether input/output voltage levels and standby and operating currents are within specified limits. Functional tests include low/high VDD margin, VDD bump, high/low VDD speed verification, dynamic (distributed and disturbed) and static refresh, as well as a full range of algorithms and data backgrounds to verify AC parameters and cold sensitive defects. For mature product types, the COLD FINAL step may be removed through an extensive qualification process, wherein COLD-FINAL test coverage is correlated to increased coverage/guard-band in the HOT FINAL/SORT test step or in the BURN-IN test step.

Devices receive a laser mark indicating the following information: work week and year, special process designator, part type, package type and speed grade.

Devices are optically scanned by an automated scanning machine for bent leads, incorrect splay and coplanarity failures.

An unaided visual inspection is made of the leads, solder, package and mark for all devices.

A Quality Assurance monitoring program oversees the electrical and mechanical performance of all production lots. QA test programs are used to monitor the outgoing electrical quality of shippable product. In the QA test programs, all parametric and functional testing is conducted at datasheet specified temperatures. Parametric tests are performed to detect opens, shorts, and input/output leakage and to determine whether input/output voltage levels, and standby and operating currents are within specified limits. Functional tests include low/high VDD margin, VDD bump, high/low VDD speed verification, dynamic (distributed and disturbed) and static refresh, as well as a full range of array exercising algorithms. These algorithms are run with datasheet specified voltage levels and timing parameters with varied data backgrounds to verify AC parameters and to identify any temperature, timing, voltage, or pattern sensitive defects.

In preparation for shipping, devices may be placed in trays or packaged on tape-and-reel. All products are dry-packed in vacuum-sealed, static-shielded bags with a desiccant.

Devices are shipped maintaining lot identity.

Figure 27: Test Process Flow — Packaged Parts

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